Department of Electronics and Telecommunication Engineering

COEP Technological University

(A Unitary Public University of Government of Maharashtra)

Time Table

Class : F. Y. M. Tech VLSI Design Academic Year : 2024 - 2025

With Effect From : 10.02.2025 Term : II (Second)

Day / TIME	9.30 am To 10.30 am	10.30 am To 11.30 am	11.30 am To 12.30 pm	12.30 pm To 1.30 pm	1.30 pm To 2.30 pm	2.30 pm To 3.30 pm	3.30 pm To 4.30 pm	4.30 pm To 5.30 pm	5.30 pm To 6.30 pm
MON		**VLSI PD Lab** (VVI) VLSI Lab			**RFCD** (MSS) ETSH - 201	**RFCD** (MSS) ETSH - 201			
TUE		**VLSI PD** (VVI) ETSH - 201	**VLSI PD** (VVI) ETSH - 201		**Verification** (AG) ETSH - 201	**Verification** (AG) ETSH - 201			
WED	**IOC** ()	**VLSI Testing** (VVI) ETSH - 201	**VLSI Testing** (VVI) ETSH - 201		**RFCD** (MSS) ETSH - 201	**Analog IC** (VSA) ETSH - 201			
THU	**IOC** ()	**Analog IC** (VSA) ETSH - 201	**Analog IC** (VSA) ETSH - 201		**VLSI PD Tut** (VVI) ETSH - 201	**Verification Lab** (AG) PG Lab - 1			
FRI	**IOC** ()	**Analog IC Lab** (VSA) VLSI Lab			**VLSI Testing** (VVI) ETSH - 201	**Mini-project** (VVI) ETSH - 201			

VLSI Physical Design (VLSI PD)(Th+Lab+Tut): Dr. (Mrs.) V. V. Ingale**, Mini-project (Lab):** Dr. (Mrs.) V. V. Ingale
Verification using SV and UVM (Verification) (Th + Lab): Ashlesha Gokhale,
Analog IC Design (Analog IC)(Th + Lab): Dr. Mrs. V. S. Agarwal,
Program Specific Elective – II: VLSI Testing (Th): Dr. (Mrs.) V. V. Ingale,
Program Specific Elective – III: RF Circuit Design (RFCD): Mr. M. S. Soman

In-charge, Timetable Committee,
Department of Electronics & Telecommunication Engineering