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**COEP Technological University Pune**

**(A Unitary Public University of Govt. of Maharashtra)**

**NEP 2020 Compliant**

Proposed Curriculum Structure

**M. Tech.**

**Electronics – VLSI Design**

**(Effective from: A.Y. 2024-25)**

**PG Program [M. Tech. Electronics – VLSI Design]**

**Proposed Curriculum Structure**

**w. e. f AY 2024-25**

**Program Outcomes (PO)**

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| --- | --- |
| PO 1 | Demonstrate higher level of professional skills to tackle multidisciplinary and complex problems related to VLSI System Design. |
| PO2 | Comprehend the state of the art VLSI technologies |
| PO3 | Characterize and design Analog, Digital, RF and Mixed signal subsystems meeting given constraints under deep sub micron environment |

**PG Program [M. Tech. Electronics – VLSI Design]**

**Proposed Curriculum Structure**

**Semester I**

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| **Sr.**  **No.** | **Course**  **Category** | **Course Code** | **Course Name** | **Teaching Scheme** | | | | **Credits** |
| **L** | **T** | **P** | **S** |
| 1. | PSMC | PSMC-01 | Graph , Field and Ring Theory for Security and Physical design | 3 | -- | -- | 1 | 3 |
| 2. | PSBC | PSBC-01 | RTL Simulation and Synthesis | 3 | 1 | 2 | 2 | 5 |
| 3. | PCC | PCC-01 | Digital IC Design | 3 | -- | 2 | 2 | 4 |
| 4. | PCC | PCC-02 | IC Fabrication Techniques | 2 | 1 | -- | -- | 3 |
| 5. | AEC | AEC-01 | Seminar | -- | -- | 2 | 2 | 1 |
| 6. | PEC | PEC-01 | Program Specific Elective –I   1. Next generation computer Architectures 2. Machine Learning 3. SoC architecture 4. Memory Technologies 5. MEMS | 3 | -- | -- | 1 | 3 |
| 7. | MLC | MLC-01 | Research Methodology and Intellectual Property Rights | -- | -- | -- | 2 | 2 |
| 8. | MLC | MLC-02 | Effective Technical Communication Skills | -- | -- | -- | 1 | 1 |
| **Total** | | | | **14** | **02** | **06** | **11** | **22** |

**Semester II**

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| **Sr.**  **No.** | **Course**  **Category** | **Course Code** | **Course Name** | **Teaching Scheme** | | | | **Credits** |
| **L** | **T** | **P** | **S** |
| 1. | OE | OE-01 | Open Elective( to be offered to other dept) | 3 | -- | -- | 1 | 3 |
| 2. | PCC | PCC-03 | Analog IC Design | 3 | -- | 2 | 1 | 4 |
| 3. | PCC | PCC-04 | Verification using SV and UVM | 2 | -- | 2 | -- | 3 |
| 4. | PCC | PCC-05 | VLSI Physical Design | 2 | 1 | 2 | -- | 4 |
| 5. | PEC | PEC-02 | Program Specific Elective –II   1. VLSI Testing 2. VLSI architectures for Signal Processing 3. Hardware / Software Co-design 4. Mixed Signal Circuit Design 5. Device Modeling | 3 | -- | -- | 1 | 3 |
| 6. | PEC | PEC-03 | Program Specific Elective –III   1. Advanced VLSI Design 2. Nano-electronic material and devices 3. Hardware Security 4. RF Circuit Design | 3 | -- | -- | 1 | 3 |
| 7. |  |  | Mini project | -- | -- | 2 | 2 | 1 |
| 8. | CCA | CCA-01 | Liberal Learning Course | -- | -- | 2 | 2 | 1 |
| **Total** | | | | **16** | **01** | **10** | **08** | **22** |

* Exit option to qualify for **PG Diploma in VLSI Design**:
  + Eight weeks domain specific industrial internship in the month of June-July after successfully completing first year of the program.

**Semester-III**

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| **Sr.**  **No.** | **Course**  **Category** | **Course**  **Code** | **Course Name** | **Teaching Scheme** | | | | **Credits** |
| **L** | **T** | **P** | **S** |
| 1. | VSEC | VSEC-01 | Dissertation Phase – I | -- | -- | 18 | 12 | 9 |
| 2. | SLC | SLC-01 | Massive Open Online Course –I | 3 | -- | -- | 3 | 3 |
| **Total** | | | | **3** | **--** | **18** | **15** | **12** |

**Semester-IV**

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| **Sr.**  **No.** | **Course**  **Category** | **Course**  **Code** | **Course Name** | **Teaching Scheme** | | | | **Credits** |
| **L** | **T** | **P** | **S** |
| 1. | VSEC | VSEC-02 | Dissertation Phase – II | -- | -- | 18 | 12 | 9 |
| 2. | SLC | SLC-02 | Massive Open Online Course –II | 3 | -- | -- | 3 | 3 |
| **Total** | | | | **3** | **--** | **18** | **15** | **12** |

* **MOOC Courses Identified:**
* Real Time Embedded Systems
* VLSI design for Fault Tolerance and Testability
* Parallel Computing
* Advanced IOT Applications

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| |  |  | | --- | --- | | **[ ] Graph , Field and Ring Theory** | | | **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks | | **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand the various types of graphs, graph properties and give examples for the given property 2. Model the given problem from their field to underlying graph model. 3. Proceed to solve the problem either through approximation algorithm or exact algorithm depending on the problem nature. 4. Appreciate the applications of digraphs and graphs in various communication networks. 5. Appreciate the applications of graphs and digraphs in various other fields. | | | Directed graphs: some standard definitions and examples of strongly, weakly, unilaterally connected digraphs, strong components and deadlock. Matrix representation of graph and digraphs. Some properties (proof not expected). Eulerian graphs and standard results relating to characterization of Eulerian graphs. Hamiltonian graph-standard theorems (Dirac theorem, Chavtal theorem, closure of graph). Non Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems.  Chromatic number; vertex chromatic number of a graph, edge chromatic number of a graph (only properties and examples)-application to colouring. Planar graphs, Euler’s formula, maximum number of edges in a planar graph, some problems related to planarity and non-planarity, Five colour theorem, Vertex Covering, Edge Covering, Vertex independence number, Edge independence number, relation between them and number of vertices of a graph.  Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs). Tournaments, some simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs.  DFS-BFS algorithm, shortest path algorithm, Min-spanning tree and Max-spanning tree algorithm, Planarity algorithm. Flows in graphs; Maxflow mincut theorem, algorithm for maxflow. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples. | | | **Reference Books :**   * J.A. Bondy and U.S.R.Murthy, “Graph Theory with Applications”, Macmillan, London, 1976, EBook, Freely Downloadable. * Cormen, Leiserson, Rivest and Stein, “Introduction to Algorithms”, 2nd Edition, McGraw-Hill, 2001. * M.Gondran and M.Minoux, “Graphs and Algorithms”, John Wiley, 1984. * H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999. | | |

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| **RTL Simulation and Synthesis** | |
| **Teaching Scheme**  Lectures: 3 hrs/week | **Examination Scheme**  Continuous evaluation - Assignments/Quizzes – 40 marks  End-Sem Exam – 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to:   1. Understand Finite State machines, RTL design and STA 2. Design IP and prototyping using Low power design techniques. 3. Use EDA tools like Cadence, Mentor Graphics and Xilinx | |
| **Syllabus Contents:**  Top down approach, Hardware modelling of combinational and sequential circuits with Verilog HDL, writing a test bench  Design of finite state machines (Synchronous and asynchronous), system design using ASM chart, Static Timing analysis, Meta-stability, clock issues, Data path and Control path design, , Arithmetic implementation strategies for data path design, Processor Design, Micro-programmed control design, Single cycle MMIPS  Programmable Logic Devices: Fine grained and coarse grained FPGA , Xilinx series  IP and Prototyping. | |
| **References:**   1. Stephen Brown and ZvonkoVranesic, “Fundamentals of Digital logic with Verilog Design”, Mc-GrawHill, 3rd edition 2. Donald D Givone, “Digital principles and Design”, Tata Mc-Graw Hill 3. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann. 4. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx 5. Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog”, Doone Publications. 6. IEEE standard HDL based on Verilog HDL, published by IEEE. 7. Ben Cohen, “Real Chip design and Verification using Verilog and VHDL”, VhdlCohen Publishing | |
| **RTL Simulation and Synthesis Lab** | |
| **Teaching Scheme**  Practical: 2 hrs/week | **Examination Scheme**  Term-work: 50 Marks  Practical: 50 Marks |
| **Laboratory Outcomes:**  At the end of the laboratory work, students will demonstrate the ability to:   1. Understanding the programmable and reprogrammable systems. 2. Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools. 3. Use EDA tools like Xilinx, Quartus II and Mentor Graphics   **Journal Submission** is in the form of CD. It should contain HDL codes, snapshot of results, synthesis reports, RTL view. In case the programs are downloaded on FPGA / SoC, the pre & post synthesis and implementation reports should also be submitted.  **List of Experiments:**  EDA tools : Xilinx / Quartus II and Mentor Graphics  Verilog implementation of   1. Mux/De-mux, Full Adder, 8-bit magnitude comparator, encoder/ decoder, priority encoder, D FF, 4 bit Shift registers (SISO, SIPO, PISO, bidirectional), Synchronous Counters, binary to gray converter, parity generator. 2. Sequence generator / detectors, Synchronous FSM – Mealy and Moore machines. 3. Vending machines - Traffic Light controller, ATM, elevator control. 4. Interfacing with peripherals like seven segment display, LED, UART, Custom GPIO, Temp sensor, Ethernet DDR. 5. SPI, I2C, PCI protocols, Bus Arbiter, UART 6. Image processing algorithms such as filtering, compression, Image enhancement   resizing of Image etc   1. Single port SRAM, Synchronous and Asynchronous FIFO 2. MIPS ( Microprocessor without interlock pipeline stages) design 3. Lab based on physical design (STA) | |

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| **[ ] Digital IC Design** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Interpret the working, construction and modeling of long channel and short channel MOS Transistors. 2. Design/ formulate / estimate combinatorial circuit for RC delay, Logic effort delay and low power in standard cell design. 3. Analyze the timing constraints in CMOS latches, registers and flip-flops. | |
| Introduction to VLSI, Energy band diagram of MOS Capacitor, Operation and working of MOS Transistor, Threshold voltage equation, Secondary effects in MOSFETS.  Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process, High–k, Metal Gate Technology, FinFET, stick diagram, IC layout design and tools. MOS capacitances, Modeling of MOS transistors using SPICE level I and II equations. Electrical wire models, SPICE wire models.  Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay. CMOS inverter: Switching Threshold, Noise Margin, Dynamic behavior of CMOS inverter, propagation delay of Inverter, RC Delay.  Combinational logic: Static CMOS design, Pass transistor logic, transmission gate logic, Logic effort delay, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, standard cell design, sizing of gates, estimating and optimizing delay in standard cell and clock distribution networks.  Sequential logic: Timing Constraints in CMOS latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master slave edge-triggered register, Dynamic latches and registers, STA and max and min delay constraints for Flip-flop.  Adder subsystem design | |
| **Reference Books :**   * N. Weste and D. Harris, “CMOS VLSI Design A Circuits and Systems Perspective”, 4th edition, Pearson. * J M Rabaey, A. Chandrakasan, B. Nikolic, “Digital Integrated Circuits A Design Perspective”, Pearson. * Sung Mo Kang, Yusuf Leblebici, “CMOS digital integrated circuits”, TataMcGraw Hill Publication * Baker Li Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition. | |

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| **[ ] IC Fabrication Techniques** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Appreciate the various techniques involved in the VLSI fabrication process. 2. Understand the different lithography methods, etching process deposition and diffusion mechanisms. 3. Analyze the fabrication of NMOS, CMOS memory and bipolar devices. | |
| Electron grade silicon. Crystal growth. Wafer preparation. Vapour phase and molecular beam epitaxy. SOI. Epitaxial evaluation. Oxidation techniques, systems and properties. Oxidation defects.  Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.  Deposition process and methods. Diffusion in solids. Diffusion equation and diffusion mechanisms.  Ion implantation and metallization. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition.  Process flow for NMOS, PMOS, CMOS, BICMOS ICs, Novel MOS and GaN based devices.  Analytical and assembly techniques. Packaging of VLSI devices. | |
| **Reference Books :**   * S.M.Sze, “VLSI Technology”, 2nd Edition , McGraw Hill, 1988 * W. Wolf, “Modern VLSI Design”, 3rd Edition, Pearson, 2002 * C.Y. Chang and S.M.Sze, “ULSI Technology”, McGraw Hill ,1996. * James D. Plummer , “Silicon VLSI Technology: Fundamentals, Practice and Modelling”, Pearson Education, 2000 | |

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| **[ ] Digital IC Design Lab** | |
| **Teaching Scheme**  Practical: 2 hrs./week | **Examination Scheme**  Marks=100  Credit = 01 |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Interpret the behavior of MOS Transistor with the help of SPICE tools. 2. DC and Transient analysis of CMOS Inverter. 3. Design of digital circuits, clock and buffer distribution networks for standard cell design according to design specs provided. | |
| List of Practical   1. DC analysis of NMOS and PMOS Transistor using NGSPICE. Estimate ION, IOFF, S and λ for 180nm / 130nm / 90nm channel length transistors. 2. Vth analysis of NMOS and PMOS Transistor using various methods. 3. DC and Transient analysis of CMOS Inverter using NGSPICE. Estimate VIL, VIH, VOL, VOH, NML, NMH from DC analysis and tpHL, tpLH from transient analysis. 4. Design of 5 stage and 7 stage ring oscillator using NGSPICE. Estimate fosc. 5. Schematic design of CMOS Inverter and its DC, Transient analysis using Cadence EDA Tool. 6. Schematic to Symbol generation using Cadence EDA Tool. 7. Schematic to Layout of CMOS Inverter using Cadence EDA Tool. 8. Post Layout simulation of CMOS Inverter and Parasitic Extraction. 9. Design of all basic gates and /or combinatorial circuits using Cadence EDA Tool. 10. Design of a 6 Transistor SRAM cell using Cadence EDA Tool. Estimate CR and PR. 11. Design of Sequential circuits using Cadence EDA Tool. | |

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| **[ ] Seminar** | |
| **Teaching Scheme**  Lectures: 2 hrs./week | **Examination Scheme**  Continuous quizzes and examination |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Identify contemporary topics/concepts pertaining to VLSI design and prepare documentation with improved substance. 2. Present the selected topic with superiority demonstrating good communication skills. | |
| Guidelines:  Selection of Topic:  - Select a topic relevant to the stream of study with content suitable for M. Tech. level presentation. For selection topics refer internationally reputed journals. The primary reference should be published during the last two or three years.  - Some of the journals/publications suitable for reference are: IEEE/the IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication - Networking and Security, Robotics and Control Systems, Signal Processing and Analysis, Machine Learning, IoT and any other related domain - Get the topic approved by the seminar guide well in advance.  Preparation of Presentation and Report:  - In slides, list out key point only. You may include figures, charts equations tables etc. but not running paragraphs. Font size used should be at least 20.  - Figures should be very clear and possibly drawn by you using suitable software tools. There should be a slide on “Conclusion”.  - A report of the seminar should be prepared which should contain the following.   * Title of the seminar. * Name and other details of presenter and the guide. * Abstract of the topic. * Contents such as Introduction, Theory to elaborate the concept, Implementation if carried out by the presenter/or fellow researcher/s, Comparison with other relevant techniques, Conclusion etc. * List of references strictly in IEEE format.   Oral Presentation: - Student needs to orally present the topic for 20 minutes with good voice projection and with modest pace  Answering Queries: - Student needs to answer queries raised by the audience and evaluators. This session shall be restricted to 5 minutes. In case of more queries, student is supposed to solve the queries offline. | |

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| **[ ] Next Generation Computer Architectures** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand the processors micro-architectural design 2. Assess performance of various architectures with respect to certain parameters 3. Identify cache and memory related issues in multi-processors 4. Understand the concept of Graphics Processor and secure processor architecture | |
| Processor design: Principles of pipeline, In order and out of order pipelines, The stages as fetch, decode, Execute etc.,  Graphics processor: Traditional GPUs, architecture of GP-GPU  Memory system: Cache memory, virtual memory, advanced Cache design, maim memory, DRAM timings, memory controller  Multicore system: Parallel programming, issues with parallel hardware  Secure processor architecture: Data encryption, Hashing, hardware security, side channel attacks  Architectures for machine learning: Basics of deep learning, design f CNN, memory organization | |
| **Reference Books :**   * Smruti R. Sarangi , “Next-Gen Computer Architecture: Till the End of Silicon” * David A. Patterson, John L. Hennessy , “Computer Organization and Design THE HARDWARE/SOF TWARE I NTERFACE” fifth edition, Morgan Kaufmann * David Harris, Sarah Harris, “ Digital Design and Computer Architecture”, Morgan Kaufmann | |

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| **[ ] Machine Learning** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand popular ML algorithms with their associated mathematical foundations 2. Understand Role of data in solving real time problems using machine learning algorithm 3. Implement basic algorithms using basic machine learning libraries mostly in python | |
| Introduction to ML: role of machine learning in computer science and problem solving, features), linear transformations, matrix vector operations in the context of data and representation, Classification and regression, Probability distribution in the context of data, Bayes rule, Supervised and unsupervised learning,  Fundamentals of ML: PCA and Dimensionality Reduction, Nearest Neighbours and KNN, Linear Regression, Decision Tree Classifiers, Concept of Generalization and concern of Overfitting, Concept of Training, Validation and Testing;  Algorithms to study: Ensembling and RF, Linear SVM, K Means, Logistic Regression , Naive Bayes  Neural Network Learning: Role of Loss Functions and Optimization, Gradient Descent and Perceptron/Delta Learning, MLP, Backpropagation MLP for Classification and Regression, Regularisation, Introduction to Deep Learning , CNNs | |
| * Tom M. Mitchell- Machine Learning- McGraw Hill Education, International Edition * Christopher M. Bishop Pattern Recognition and Machine Learning- Springer, 2nd edition | |

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| **[ ] SoC architecture** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand fundamentals of designing system-on-chip 2. Analyze the basics of system on chips 3. Analyze the communication architecture | |
| Memory, Bus protocols: UART, I2C, AXI/AHB, AMBA, PCI | |
| * Introduction: Trends in Computer Systems, SoC definition, benefits, challenges * SoC Components : Processing units (CPU, Accelerators, IPs),Memory and peripherals , On-chip interconnect * SoC-Implementation(ASIC, FPGAs): VLSI design overview, FPGA overview and Implementation on FPGA with Xilinx/Intel, * OS & Software Integration: OS Basics, resource management, multithreading Linux installation and configuration on a FPGA SoC * System-Level Design: Models of computation, SystemC overview Transaction-Level Modeling (initiators, transactors) * SoC Verification : Overview of verification techniques, Verification flow Verification tools (UVM, SCV), Case Studies * SoC Security : HW/SW Multi-Level Security, Overview of hardware security, IP protection, Encryption | |
| * Reference books | |

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| **[ ] MEMS** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand the Micro fluidic Principles and study its applications. 2. Learn the applications of Sensors in Health Engineering. 3. Learn the principles of Micro Actuators and Drug Delivery system 4. Learn the Micromachining Processes 5. Learn the design and applications of RF MEMS inductors and capacitors. 6. Learn about RF MEMS Filters and RF MEMS Phase Shifters. | |
| Bio-MEMS  Introduction-The driving force behind Biomedical Applications – Biocompatibility - Reliability Considerations-Regularity Considerations – Organizations - Education of Bio MEMS-Silicon Micro fabrication-Soft Fabrication techniques  Micro fluidic Principles- Introduction-Transport Processes- Electro kinetic Phenomena-Micro valves Micro mixers- Micro pumps.  SENSOR PRINCIPLES and MICRO SENSORS: Introduction-Fabrication-Basic Sensors-Optical fibers-Piezo electricity and SAW devices-Electrochemical detection-Applications in Medicine  MICRO ACTUATORS and DRUG DELIVERY: Introduction-Activation Methods-Micro actuators for Micro fluidics-equivalent circuit representation-Drug Delivery  RF-MEMS  Micromachining Processes - methods, RF MEMS relays and switches. Switch parameters. Actuation mechanisms. Bistable relays and micro actuators. Dynamics of switching operation.  MEMS inductors and capacitors. Micro-machined inductor. Effect of inductor layout. Modelling and design issues of planar inductor. Gap-tuning and area-tuning capacitors. Dielectric tunable capacitors.  MEMS phase shifters. Types. Limitations. Switched delay lines. Fundamentals of RF MEMS Filters.  Micro-machined transmission lines. Coplanar lines. Micro-machined directional coupler and mixer.  Micro-machined antennas. Microstrip antennas – design parameters. Micromachining to improve performance. Reconfigurable antennas. | |
| * Steven S. Saliterman, “Fundamentals of Bio MEMS and Medical Micro devices”, Wiley Inter science, 2006. * Vijay. K. Varadan, K.J. Vinoy, and K.A. Jose, “RF MEMS and their Applications”, Wiley India, 2011. * Albert Folch , “Introduction to Bio MEMS”, CRC Press, 2012 * Gerald A. Urban, “Bio MEMS”, Springer, 2006 * Wanjun wang, steven A. Soper, “Bio MEMS”, 1st Edition, CRC Press, 2006. * M. J. Madou, “Fundamental of Micro fabrication”, 2nd Edition, CRC Press, 2002. * G.T. A. Kovacs, “Micro machined Transducers Sourcebook”, 1st Edition, McGraw Hill, 1998. * Recent literature in Bio MEMS. * H. J. D. Santos, “RF MEMS Circuit Design for Wireless Communications”, Artech House, 2002. * G. M. Rebeiz, “RF MEMS Theory, Design, and Technology”, Wiley, 2003. * Recent literature in RF MEMS. | |

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| **[ ] Research Methodology and Intellectual Property Rights** | |
| **Teaching Scheme**  Lectures: 2 hrs./week | **Examination Scheme**  Continuous quizzes and examination |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand research problem formulation and approaches of investigation of solutions for research problems 2. Learn ethical practices to be followed in research and apply research methodology in case studies and acquire skills required for presentation of research outcomes 3. Discover how IPR is regarded as a source of national wealth and mark of an economic leadership in context of global market scenario 4. Summarize that it is an incentive for further research work and investment in R & D, leading to creation of new and better products and generation of economic and social benefits | |
| Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations.  Effective literature studies approaches, analysis Use Design of Experiments /Taguchi Method to plan a set of experiments or simulations or build prototype Analyze your results and draw conclusions or Build Prototype, Test and Redesign  Plagiarism, Research ethics Effective technical writing, how to write report, Paper. Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee  Introduction to the concepts Property and Intellectual Property, Nature and Importance of Intellectual Property Rights, Objectives and Importance of understanding Intellectual Property Rights  Understanding the types of Intellectual Property Rights: -Patents-Indian Patent Office and its Administration, Administration of Patent System – Patenting under Indian Patent Act, Patent Rights and its Scope, Licensing and transfer of technology, Patent information and database. Provisional and Non Provisional Patent Application and Specification, Plant Patenting, Idea Patenting Integrated Circuits, Industrial Designs, Trademarks (Registered and unregistered trademarks), Copyrights, Traditional Knowledge, Geographical Indications, Trade Secrets, Case Studies  New Developments in IPR, Process of Patenting and Development: technological research, innovation, patenting, development International Scenario: WIPO, TRIPs, Patenting under PCT | |
| Reference Books:   * Aswani Kumar Bansal, “Law of Trademarks in India” * B L Wadehr, “Law Relating to Patents, Trademarks, Copyright, Designs and Geographical Indications” * G.V.G Krishnamurthy, “The Law of Trademarks, Copyright, Patents and Design” * Satyawrat Ponkse, “The Management of Intellectual Property” * S K Roy Chaudhary & H K Saharay, “The Law of Trademarks, Copyright, Patents” * T. Ramappa, S. Chand, “Intellectual Property Rights under WTO” * Manual of “Patent Office Practice and Procedure” * WIPO: “WIPO Guide To Using Patent Information” * Halbert , “Resisting Intellectual Property”, Taylor & Francis * Mayall , “Industrial Design”, Mc Graw Hill * Niebel, “Product Design”, Mc Graw Hill * Asimov , “Introduction to Design”, Prentice Hall * Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age” | |

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| **[ ] Effective Technical Communication Skills** | |
| **Teaching Scheme**  Lectures: 2 hrs./week | **Examination Scheme**  Continuous quizzes and examination |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Produce effective dialogue for business related situations 2. Use listening, speaking, reading and writing skills for communication purposes and attempt tasks by using functional grammar and vocabulary effectively 3. Analyze critically different concepts / principles of communication skills 4. Demonstrate productive skills and have a knack for structured conversations 5. Appreciate, analyze, evaluate business reports and research papers | |
| Fundamentals of Communication: 7 Cs of communication, common errors in English, enriching vocabulary, styles and registers  Aural-Oral Communication: The art of listening, stress and intonation, group discussion, oral presentation skills  Reading and Writing: Types of reading, effective writing, business correspondence, interpretation of technical reports and research papers | |
| Reference Books:   * Raman Sharma, “Technical Communication”, Oxford University Press. * Raymond Murphy, “Essential English Grammar” (Elementary & Intermediate) Cambridge University Press * Mark Hancock, “English Pronunciation in Use”, Cambridge University Press * Shirley Taylor, “Model Business Letters, Emails and Other Business Documents”, Prentice Hall, Seventh Edition * Thomas Huckin, Leslie Olsen, “Technical writing and Professional Communications for Non-native speakers of English”, McGraw Hill | |

**Semester II**

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| **[ ] Analog IC Design** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Interpret the graphical techniques for modeling Analog circuits and MOS transistor small geometry effects. 2. Design / formulate / estimate Analog sub circuits and cascaded stages for current and voltage gain, input and output impedances and frequency response. 3. Articulate the knowledge of analog sub circuits to design OP AMPS | |
| **Foundation:** Analog Landscape, Techniques for intuitive and graphical understanding of analog circuits viz R, L, C and dependent V and I sources and their combinations, Large Signal and Small Signal Models of MOS Transistors.  **Analog Sub-circuits:** Stability, Operating point Analysis and Design, estimation of voltage gain, input resistance, output resistance for Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascode stage, Current Mirror.  **Differential Amplifiers:** Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell. Cascade current mirrors, Active current mirrors.  **Frequency response:** Fundamental concepts, Bode rules, Miller theorem, CS stage, Source follower, Common gate stage, Cascade stage and difference pair, Noise analysis  **Operational amplifiers design:** One stage OPAMP, Two stage OPAMP, Gain boosting, Slew rate, PSRR. Design equations and procedure  **Advanced OPAMP:** Cascode and folded cascode op-amps, common mode feedback techniques  Bandgap References, Introduction to Switched Capacitor Circuits, Nonlinearity and Mismatch. | |
| **Reference Books :**   * Behzad Razavi, “Fundamentals of Microelectronics”, Wiley, 3rd edition, 2021. * Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Mc Graw-Hill, 2nd edition, 2018. * Allen Holberg, “CMOS analog Circuit Design”, Oxford University Press, 3rd edition, 2017 . * Donald Neamen, “Microelectronics Circuit Analysis and Design”, McGraw Hill, 4th Edition, 2021. * Jacob Millman, Christos C Halkias, Chetan D Parikh, “Integrated Electronics”, Mc Graw Hill Education, 2nd Edition, 2017 | |

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| **[ ] Verification using SV and UVM** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Learn verification techniques and create reusable verification environment. 2. Verify increasingly complex designs more efficiently. 3. Apply the concepts of testing to get a better yield in IC design 4. Use EDA tools like Cadence, Mentor Graphics. | |
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| **Verification guidelines:** Basic Test bench functionality, Directed testing, Verification Process, T est bench components, Constrained-Random stimulus, Functional coverage, Building layered test bench, Simulation environment phases, Maximum code reuse, Test bench performance.  **System Verilog Constructs:** Primitive test bench methodology, Importance of verification and its guidelines, Verification plan, System Verilog constructs  **Data types:** Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Array methods,  **Procedural Blocks:** Fork Join, Tasks and Functions  **Inter Process Communication**: Semaphore, mailbox  **Interface:** ports, clocking blocks, virtual interface Top-level Program – Module interactions.  **Basic OOPs:** Inheritance, Polymorphism Randomization: Randomization and constrained Randomization, pre\_randomize and post\_randomize functions, Random number generators  **Code and Functional coverage:** Cover group, cover points, Bins  **System Verilog Assertions**: Properties, Boolean expressions  Introduction to UVM methodology | |
| **Reference Books :**   1. Chris Spears, “ System Verilog for Verification”, Springer, 2nd Edition 2. Janick Bergeron, “ Writing test benches l functional verification of HDL models”, Kluwer Academic Publishers 3. IEEE 1800-2009 standard (IEEE Standard for SystemVerilog— Unified Hardware Design, Specification and Verification Language). 4. System Verilog website – [www.systemverilog.org](http://www.systemverilog.org) 5. OVM, UVM(on top of SV) [www.verificationacademy.com](http://www.verificationacademy.com) | |

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| **[ ] VLSI Physical Design** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand the concepts of Physical Design Process such as partitioning; Floor planning, Placement and Routing. 2. Discuss the concepts of design optimization algorithms and their application to physical design automation. 3. Understand the concepts of simulation and synthesis in VLSI Design Automation 4. Formulate CAD design problems using algorithmic methods | |
| VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.  Layout compaction, placement and routing. Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.  Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.  Simulation and logic synthesis- gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.  High-level synthesis- hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations. | |
| Reference Books:   * S.H. Gerez, “Algorithms for VLSI Design Automation”, John Wiley (India), 2006. * N.A.Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer, 2012. * S.M. Sait, H. Youssef, “VLSI Physical Design Automation”, Cambridge India, 2010. * M.Sarrafzadeh, “Introduction to VLSI Physical Design”, McGraw Hill (IE), 1996. * Giovanni De Micheli, “Synthesis and Optimization of Digital Circuits”, McGraw Hill, 2017. | |

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| **[ ] Analog IC Design Lab** | |
| **Teaching Scheme**  Practical: 2 hrs./week | **Examination Scheme**  Marks=100  Credit = 01 |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Interpret the behavior of MOS Transistor with the help of SPICE tools. 2. DC, AC, Noise and frequency analysis of Single stage amplifiers, current sources, differential amplifiers and two stage OPAMP. 3. Solve analog design problems by changing the design parameter of the circuit with the help of Cadence Virtuoso. | |
| List of Practical   1. DC analysis of NMOS and PMOS Transistor using NGSPICE. Estimate gm, gds etc. 2. AC analysis of NMOS and PMOS Transistor using NGSPICE. Estimate gm, gds etc. 3. AC analysis of Common Source Amplifier with different loads using NGSPICE. Estimate gm, gds etc. 4. AC analysis of Common Gate and Common Drain Amplifier using NGSPICE. Estimate gm, gds etc. 5. AC analysis of Current Source using NGSPICE. Estimate gm, gds etc. 6. DC and AC analysis of two stage Differential Amplifier with different loads using Cadence EDA Tool. 7. Noise and Frequency analysis of Amplifiers using Cadence EDA Tool. 8. Design of Band Gap reference circuits using Cadence EDA Tool. 9. Design of D to A converters using Cadence EDA Tool. 10. Design of A to D converters using Cadence EDA Tool. 11. Design of basic switched capacitor filters using Cadence EDA Tool. | |

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| **[ ] VLSI Physical Design Lab** | |
| **Teaching Scheme**  Practical: 2 hrs./week | **Examination Scheme**  Marks=100  Credit = 01 |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Apply the constraints posed by the VLSI fabrication technology to design automation tools using graph algorithms 2. Simulate partitioning algorithms viz., KL algorithm and simulated annealing algorithms. 3. Optimize floor planning using time driven floor planning algorithm and hierarchical tree based methods 4. Optimize routing using two terminal and multi terminal algorithms. | |
| Cycle 1:  1) Graph algorithms 1) Graph search algorithms 1) Depth first search 2) Breadth first search 2) Spanning tree algorithm 1) kruskal’s algorithm 3) Shortest path algorithm 1) Dijkstra algorithm 2) Floyd- Warshall algorithm 4) Steiner tree algorithm  2) Computational geometry algorithm 1) Line sweep method 2) Extended line sweep method  Cycle 2:  1) Partitioning algorithms 1) Group migration algorithms 1) Kernighan –Lin algorithm 2) Extensions of Kernighan-Lin algorithm 1) Fiduccias –Mattheyses algorithm 2) Goldberg and Burstein algorithm 2) Simulated annealing and evolution algorithms 1) Simulated annealing algorithm 2) Simulated evolution algorithm 3) Metric allocation method  2) Floor planning algorithms 1) Constraint based methods 2) Integer programming based methods 3) Rectangular dualization based methods 4) Hierarchical tree based methods 5) Simulated evolution algorithms 6) Time driven Floorplanning algorithms  3) Routing algorithms 1) Two terminal algorithms 1) Maze routing algorithms 1) Lee’s algorithm 2) Soukup’s algorithm 3) Hadlock algorithm 2) Line-Probe algorithm 3) Shortest path based algorithm 2) Multi terminal algorithm 1) Stenier tree based algorithm 1) SMST algorithm 2) Z-RST algorithm | |
| * Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic, 1998. * Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008. | |

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| **[ ] VLSI Testing** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to | |
| Introduction to testing: Testing philosophy, Role of testing, types of testing, Test economics, yield, rule of 10, ATE  Fault modelling: Defects , errors and faults, fault modelling-stuck at faults, bridging faults, state dependent faults, multiple faults, fault collapsing  Test pattern generation methods and algorithms: Boolean difference, path sensitization, SCOAP controllability and observability, Random test generation, D algorithm  Design for test by means of scan: making circuit testable, testability insertion, overheads of scan design  Built in self test: Boundary scan architecture, | |
| Reference Books:   * Zainalabedin Navabi, “Digital System Test and Testable Design, Using HDL Models and Architectures”, Springer * Michael L. Bushnell, Vishwani D. Agrawal, “Essentials Of Electronic Testing Fordigital, Memory And Mixed-Signal Vlsi Circuits”, Kluwer academic Publishers | |

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| **[ ] VLSI Architecture for Signal Processing** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to | |
| Introduction to digital signal processing systems: Introduction, Typical DSP algorithms, DSP applications demands and scaled technologies,  Iteration bound: Introduction, data flow graph representation, loop bound and iteration bound, Iteration bound of multirate data flow graphs  Pipelining and parallel processing: pipelining of FIR digital filters, Parallel processing, pipelining and Parallel processing for low power  Unfolding and folding: Algorithm and properties of Unfolding, Applications of Unfolding, Folding transformation, Register minimization in folded architecture  Pipelined and parallel recursive and adaptive filters: Pipelining in IIR digital filters, Parallel processing for IIR filters, Pipelined adaptive digital filtes  Programmable digital signal processors: Features of DSP processors, DSP processors for mobile and wireless communication | |
| * Keshab Parhi, “VLSI Digital Signal Processing Systems: Design and Implementation” Willey | |

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| **[ ] Hardware / Software Co-design** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand Serial and parallel communication protocols. 2. Model data flow and implement the same through software and hardware. 3. Operate data flow using USB and CAN bus for PIC microcontrollers. 4. Design embedded Ethernet for Rabbit processors. 5. Design CORDIC and Crypto coprocessor. | |
| The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design.  Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.  Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.  Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph, Transistor Structures, Construction of the Data Flow Graph.  Finite State Machine with Datapath: Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Datapath, FSMD Design Example: A Median Processor.  System on Chip: The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoC Modeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co-Processor. | |
| * Patrick Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer, 2010. * Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998. | |

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| **[ ] Mixed Signal Circuit Design** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Appreciate the fundamentals of data converters and also optimized their performances. 2. Understand the design methodology for mixed signal IC design using gm/Id concept. 3. Analyze the design of current mirrors and operational amplifiers 4. Design the CMOS digital circuits and implement its layout. 5. Design the frequency and Q-tunable time domain filters. | |
| Concepts of Mixed-Signal Design and Performance Measures. Introduction and Principle behind ADC’s and DAC’s - Performance Metrics of ADCs and DACs, Nyquist Rate DACs, Sample-and-Hold Circuits, Comparators- Characterization – Two stage comparators – open loop comparators, Nyquist rate ADCs: Flash, SAR, Pipelined, Time-interleaved ADCs. Overview of oversampling ADCs.  Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model , Limitations of the Second-Order Small-Signal Model, PLL characterization and Design Example. Jitter and Phase Noise, Period Jitter , P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators , LC Oscillators, phase Noise of Oscillators, jitter and Phase Noise in PLLs.  Design methodology for mixed signal IC design using gm/Id concept.  Design of Current mirrors. References. Comparators and Operational Amplifiers.  CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations.  Design of frequency and Q tunable continuous time filters. | |
| * David A. Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley and Sons, 1997. * B. Razavi, “Principles of Data Conversion System Design”, Wiley-IEEE Press, 1St Edition, 1994. * R. J. Baker, “CMOS Mixed Signal circuit Design”, Wiley-IEEE Press, 2nd Edition, 2008. * M.Gustavsson, J. J. Wikner, and N. N. Tan, “CMOS Data Conversion for Communications”, Springer; 2000 | |

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| **[ ] Device Modelling** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to | |
| MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson’s Equation, CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges.  The MOS transistor: Small signal modelling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.  The bipolar transistor: Ebers-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics  Compact Modeling: Compact model Level 1, Level 2, Level 3, UTB/FD SOI MOSFET, FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices. | |
| * S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981. * M. Lundstrom, Fundamentals of Nanotransistors, World Scientific Publishing Co Pte Ltd 2017. * Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987. * E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995. * J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009 | |

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| **[ ] Advanced VLSI Design** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand Low power design techniques | |
| Low Power design Techniques: Major component of power dissipation, Threshold voltage scaling, Impact of scaling on dynamic power, circuit topologies for low power, Leakage power contributors and remedies, Low power design technique, DVFS, pipelining, parallel processing.  Low Power Memory Design: Transistor Scaling and leakage, leakage control, Circuit level leakage reduction techniques, MTCMOS, SCCMOS, VTCMOS, DTMOS, Cache Memories leakage, Noise margin, Parametric Failures in SRAM, SRAM leakage reduction schemes, Supply gating, Iddq test, Stuck at fault tests, test power, test coverage, gated de-cap.  Interconnect: Capacitive Parasitics, Resistive Parasitics, Inductive parasitic, Electrical wire model of Transmission Line, advanced interconnect techniques. | |
| Reference Books:   * Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000. * J M Rabaey, A. Chandrakasan, B. Nikolic, “Digital Integrated Circuits A Design Perspective”, Pearson. | |

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| **[ ] Nano-electronic material and devices** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand the physics and materials for Nanoelectronics 2. Understand the scaling issues 3. Explain the need for non-classical and non-silicon based devices 4. Analyse the performance of novel devices | |
| Overview: Nano devices, Nano materials, Nano device characterization, Definition of Technology node, MOS capacitor, MOS Scaling theory, Moore’s Law and Koomey's law.  Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology, Role of interface quality and related process techniques, Gate oxide thickness, scaling trend, SiO2 vs High-k gate dielectrics, Integration issues of high-k, Interface states, bulk charge, band offset, stability, reliability - Qbd high field, possible candidates, CV and IV techniques, Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot, Metal gate transistor : Motivation, requirements, Integration Issues.  Non classical MOS transistor: Requirements, and Novel devices  SOI - PDSOI and FDSOI, Ultrathin body SOI - double gate transistors, integration issues.  Vertical transistors - FinFET and Cylindrical gate FET.  Novel devices: Tunnel FET, Negative-Capacitance (NC) FET.  Metal source/drain junctions - Properties of schotky junctions on Silicon, Germanium and compound semiconductors -Workfunction pinning.  Germanium Nano MOSFETs : strain , quantization , Advantages of Germanium over Silicon, PMOS versus NMOS.  Compound semiconductors - Compound semiconductors MOSFETs in the context of channel quantization and strain, Hetero structure MOSFETs, exploiting novel materials, strain, quantization.  Emerging nano materials : CNT, Graphene, Nanotubes, quantum dots, nanorods and other nano-structures. | |
| * Y. Taur and T. Ning, “Fundamentals of Modern VLSI devices” Cambridge University Press * Nicollian and J. R. Brews “MOS (Metal Oxide Semiconductor) Physics and Technology” Wiley Publishers * Brundle, C.Richard; Evans, Charles A. Jr.; Wilson, Shaun “Encyclopedia of Materials Characterization”, Elsevier. * Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017. * J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009 6. Related research papers. | |

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| **[ ] Hardware Security** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand and optimize the process of implementing cryptographic algorithm on hardware 2. Learn the different types of attacks 3. Learn and implement of crypto processor based solutions | |
| **Introduction to hardware Cryptography**: Finite Fields, AES Hardware, S-Box,  Algorithm to Hardware, Intro to ECC, Hardware Design of ECC **Introduction to Side Channel Analysis**: Advanced SCA, Introduction to Fault Attacks  Advanced Fault Attacks, Algebraic Fault Analysis Design-for-Testability for Cryptographic Designs, Introduction to Micro-architectural attacks **Types of crypto processor**: Tamper resistance cryptographic processor, Homomorphic cryptoprocessor design, Open source cryptographic processor, Reconfigurable cryptographic processor | |
| * M. Tehranipoor and C. Wang, “Introduction to Hardware Security and Trust”, Springer. * Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, “Hardware Security: Design, Threats, and Safeguards”, CRC Press * Tom St. Denis, “Cryptography for developers”, Syngress | |

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| **[ ] RF Circuit Design** | |
| **Teaching Scheme**  Lectures: 3 hrs./week | **Examination Scheme**  Test I - 20 Marks  Test II - 20 Marks  End Sem Exam - 60 marks |
| **Course Outcomes:**  At the end of the course, students will demonstrate the ability to   1. Understand the basics of RF system design and analyse the high frequency amplifier design 2. Appreciate the need for LNA and learn different LNA topologies and design techniques 3. Understand the requirement of RF Mixer, its function and performance parameters 4. Analyse the various types of synthesizers, oscillators and their characteristics. 5. Learn about the need for power amplifiers and the effects of nonlinearities | |
| Overview of RF Systems: Wireless Transmitter and Receiver Architecture – Heterodyne and Super Heterodyne Systems - Basic concepts in RF design - units in RF Design, time variance - Effects of Nonlinearity: harmonic distortion, gain compression, cross modulation, intermodulation, cascaded nonlinear stages, AM/PM conversion - Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, representation of noise in circuits.  High frequency amplifier design – Types of amplifiers: Narrowband and Wideband Amplifiers - zeros as bandwidth enhancers, shunt-series amplifier, fT doublers, neutralization and unilateralization  Need for LNA: Friis’ equation - Low noise amplifier design – LNA topologies: noise cancelling LNA topology, distortion cancelling LNA topology - linearity and large signal performance  Need for Mixers – Noise and Linearity trade-off in RF Mixer design - traditional mixer circuits: multiplier-based mixers, subsampling mixers, diode-ring mixers - Noise Folding - Single-sideband and Double-sideband Noise Figure – Feedthrough: Single balanced and Double Balanced – IP3 and IP2 improvement - Oscillators and synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers – phase noise considerations.  RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations. RFIC simulation and layout- General Layout Issues, Passive and Active Component Layout. | |
| * Thomas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, 2nd Edition, Cambridge University Press, 2004. * B. Razavi, “RF Microelectronics”, 2nd Edition, Prentice Hall, 1998. * A. Abidi, P.R. Gray, and R.G. Meyer, eds., “Integrated Circuits for Wireless Communications”, New York: IEEE Press, 1999. * R. Ludwig and P. Bretchko, “RF Circuit Design, Theory and Applications”, Pearson, 2000. * Mattuck,A., “Introduction to Analysis”, Prentice-Hall,1998. | |