Department of Electronics and Telecommunication Engineering

COEP Technological University

(A Unitary Public University of Government of Maharashtra)

Time Table

Class : **M. Tech (Electronics-VLSI & Embedded Systems)** Academic Year : 2023 - 2024

With Effect From : 05.09.2023 Term : I (First)

Day / TIME	9.00 am To 10.00 am	10.00 am To 11.00 am	11.00 am To 12.00 pm	12.00 pm To 1.00 pm	1.00 pm To 2.00 pm	2.00 pm To 3.00 pm	3.00 pm To 4.00 pm	4.00 pm To 5.00 pm
MON		**MPA - Tut** (PPB) PG Lab - II	**MPA Laboratory** (PPB) PG Lab - II			**PGFT** (VSV) ETSH – 201	**PGFT** (VSV) ETSH – 201	
TUE		**RTL** (VVI) ETSH - 201	**RTL** (VVI) ETSH – 201	**MPA** (PPB) ETSH - 201			**Seminar** (YMV) ETSH – 201	
WED		**PLES** (GKA) ETSH - 201	**RTL** (VVI) ETSH – 201	**MPA** (PPB) ETSH – 201		**RTL - Tut** (VVI)	**RTL Laboratory** (VVI) Embedded Systems Lab	
THU		**PLES** (GKA) ETSH - 201	**MPA** (PPB) ETSH – 201	**ML** (YMV) ETSH - 201	**Lunch Break**	**PGFT** (VSV) ETSH - 201	**PGFT - Tut** (VSV) ETSH - 201	
FRI		**PLES** (GKA) ETSH - 201	**PLES Laboratory** (GKA)			**ML** (YMV) ETSH - 201	**ML** (YMV) ETSH - 201	
SAT								

Probability, Graph and Field Theory (PGFT) (Th + Tut): Dr. (Mrs.) V. S. Vyas, **RTL Simulation and Synthesis (RTL) (Th + Lab + Tut):** Dr. (Mrs.) V. V. Ingale
Programming Languages for Embedded Software (PLES) (Th + Lab): Mr. G. K. Andurkar, **Machine Learning (ML) (Th):** Mrs. Y. M. Vaidya
Microcontrollers: Architecture and Programming (MAP) (Th + Lab + Tut): Dr. P. P. Bartakke, **Seminar (Lab):** Mrs. Y. M. Vaidya

In-charge, timetable committee,
Department of Electronics & Telecommunication Engineering